TEST REPORT

Engineering Recommendation G83 Issue 2 (December 2012)
Recommendations For The Connection Of Type Tested Small-Scale Embedded Generators (Up To 16A Per Phase) In Parallel With Low-Voltage Distribution Systems

Report reference No. ..... :	161008073GZU-001
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Date of issue ..... :	27 Oct., 2016
	21 pages
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Applicant's Name ..... :	Shenzhen SOFARSOLAR Co., Ltd.
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Test specification	
Standard ..... :	G83 Issue 2 : 2012
Test procedure ..... :	Type test
Non-standard test method ..... :	N/A
Test Report Form No. ..... :	G83/2a
TRF originator ..... :	Intertek
Master TRF ..... :	dated 2013-07
Test item description ..... :	AC-coupled Storage Converter
Trademark ..... :	SOFAR SOLAR
Manufacturer ..... :	Same as applicant
Factory ..... :	Same as applicant
Model and/or type reference ..... :	ME 3000SP

Rating(s)..... :	Battery Type: Lead-acid, Lithium-ion Battery Voltage Range: 42-58Vdc Max. Charging Current: 60A Max. Discharging Current: 60A Max. Charging & Discharging Power: 3000VA Nominal Grid Voltage: 230Vac Nominal output Voltage (stand-alone): 230Vac Max. output Current: 13A Nominal Grid frequency: 50Hz Power factor: 1 (adjustable +/-0.8) Ingress protection: IP65 Operating Temperature Range: -25℃ - 60℃ Protective Class: Class I

Summary of testing:

The sample(s) tested complied with the type test requirement of G83 Issue 2: 2012

Test case verdicts

Test case does not apply to the test object .:	N/A
Test item does meet the requirement .....:	P(ass)
Test item does not meet the requirement ...:	F(ail)

Testing

Date of receipt of test item .....:	10 Oct., 2016
Date(s) of performance of test .....:	10 Oct., 2016 – 25 Oct., 2016

General remarks

The test results presented in this report relate only to the object tested.
This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory.
"(See Enclosure #)" refers to additional information appended to the report.
"(See appended table)" refers to a table appended to the report.

Throughout this report a point is used as the decimal separator.

When determining the test conclusion, the Measurement Uncertainty of test has been considered.

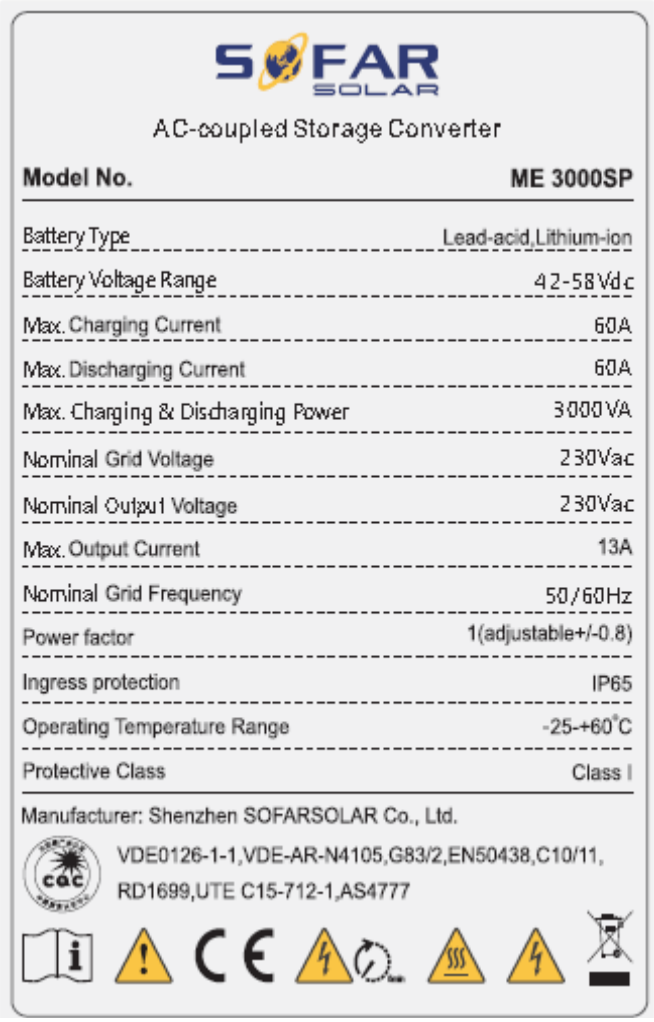
General product information:

The equipment under test is single phase energy storage inverter. They are responsible for converting the direct current generated by battery into single-phase 230V, 50 Hz. It is basic insulation between grid and battery. Two mechanical disconnection device (relay) is provided between grid and battery on line and neutral conductor

The equipments have three working mode. Charge mode, Discharge mode, Stand-alone mode :
Charge mode: The AC voltage from mains charges the battery provided in the final system.
Discharge mode: The inverter converters the energy from the battery to 230Va.c.,50 Hz voltage and connected to AC mains. In this mode the inverter works as grid connected inverter.
Stand-alone mode: The inverter converter the energy from the battery to 230Va.c.,50 Hz voltage and feed the general load. In this mode the inverter worked as stand-alone inverter.

Rate of change of frequency (RoCoF) and frequency shift detection was used for LOM protection.

Copy of marking plate:



Engineering recommendation G83/2			
Summary of testing			
Clause	Requirement – Test	Result – Remark	Verdict
5	Connection, Protection & Testing Requirements		
5.3	Interface Protection		P
5.3.1	Interface Protection Settings and Test Requirements	See table 5.3.1	P
5.3.2	Loss of Mains Protection	See table 5.3.2	P
5.3.3	Frequency Drift and Step Change Stability Test	See table 5.3.3	P
5.3.4	Automatic Reconnection	See table 5.3.4	P
5.4	Quality of Supply		P
5.4.1	Testing for Harmonic emissions	See table 5.4.1	P
5.4.2	Testing for flicker	See table 5.4.2	P
5.5	DC Injection	See table 5.5 and 5.6	P
5.6	Power Factor	See table 5.5 and 5.6	P
5.7	Short Circuit Current Contribution	See table 5.7.2	--

Appendix 1: Testing table

Table 5.3.1 Protection Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						P
Function	Setting		Trip test			
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20s	47.48 Hz	20.05s 20.05s 20.00s 20.05s 20.00s	47.7Hz 25s	No trip
U/F stage 2	47Hz	0.5s	46.96Hz	0.522 0.512 0.536 0.522 0.532	47.2Hz 19.98s	No trip
					46.8Hz 0.48s	No trip
O/F stage 1	51.5Hz	90s	51.52HZ	90.20s 90.20s 90.20s 90.00s 90.20s	51.3Hz 95s	No trip
O/F stage 2	52Hz	0.5s	52.01HZ	0.510s 0.524s 0.514s 0.524s 0.526s	51.8Hz 89.98s	No trip
					52.2Hz 0.48s	No trip
Operation of the under/over frequency protection will be demonstrated for an increase or decrease of frequency within ± 0.5% of the trip settings, e.g. for an Over Frequency setting of 50.5 Hz the permissible operating range is 50.5 ± 0.25 Hz. The test frequency should be applied in steps of ± 0.5% of setting for a duration that is longer than the trip time delay, for example 1 second in the case of a delay setting of 0.5 second.						

Appendix 1: Testing table

Table 5.3.1 (Continue) Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2						P
Function	Setting		Trip test		No trip tests	
	Voltage	Time delay	Voltage	Time delay	Voltage /time	Confirm no trip
U/V stage 1	200.1V	2.5s	201.3V	2.54s 2.53s 2.54s 2.52s 2.54s	204.1V 3.5s	No trip
U/V stage 2	184V	0.5s	185.6V	0.525s 0.515s 0.515s 0.520s 0.520s	188V 2.48s	No trip
					180V 0.48s	No trip
O/V stage 1	262.2V	1.0s	261.9V	1.01s 1.03s 1.02s 1.03s 1.01s	258.2V 2.0s	No trip
O/V stage 2	273.7V	0.5s	273.3V	0.515s 0.525s 0.505s 0.520s 0.520s	269.7V 0.98s	No trip
					277.7V 0.48s	No trip
Note for Voltage tests the Voltage required to trip is the setting ±3.45V. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting ±4V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.						

Appendix 1: Testing table

Table 5.3.2 LOSS OF MAINS TEST						P
Method used	To be carried out at three output power levels according to BS EN 62116					
Balancing load on islanded network	33% -5% Q Test 22	66% -5% Q Test 12	100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5 seconds	201.5ms	209.0ms	288.0ms	263.0ms	288.0ms	287.0ms
Note: Inverter connected to a network combining a resonant circuit with a Q factor = 1 and a variable load; the value of the load is to match the inverter output to within +/-5%. A switch is placed between inverter/load and distribution system.						

Table 5.3.3 Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6				P
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		P
Negative Vector Shift	50.5Hz	- 9 degrees		P
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	P
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	P

Table 5.3.4 Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5						P
Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.						
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.				
60s	70.2s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz	
Confirmation that the SSEG does not re-connect.		Not reconnection	Not reconnection	Not reconnection	Not reconnection	

Table 5.4.1 Harmonics			P
SSEG rating per phase (rpp)		2.9kW	NV=MV*3.68/rpp
Har	At 45-55% of rated	100% of rated output	

Appendix 1: Testing table

monic	output					
	Measured Value (MV) (mA)	Normalised Value (NV) (mA)	Measured Value (MV) (mA)	Normalised Value (NV) (mA)	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.0143	0.0181	0.0219	0.0278	1.080	
3	0.0835	0.1060	0.1033	0.1311	2.300	
4	0.0112	0.0142	0.0093	0.0119	0.430	
5	0.0323	0.0410	0.0356	0.0452	1.140	
6	0.0143	0.0181	0.0137	0.0174	0.300	
7	0.0108	0.0137	0.0279	0.0355	0.770	
8	0.0176	0.0224	0.0134	0.0170	0.230	
9	0.0206	0.0261	0.0350	0.0445	0.400	
10	0.0130	0.0165	0.0125	0.0158	0.184	
11	0.0215	0.0273	0.0416	0.0528	0.330	
12	0.0125	0.0158	0.0099	0.0125	0.153	
13	0.0235	0.0299	0.0429	0.0544	0.210	
14	0.0100	0.0127	0.0099	0.0126	0.131	
15	0.0252	0.0320	0.0425	0.0540	0.150	
16	0.0087	0.0111	0.0066	0.0083	0.115	
17	0.0248	0.0315	0.0397	0.0504	0.132	
18	0.0088	0.0112	0.0088	0.0111	0.102	
19	0.0234	0.0296	0.0363	0.0461	0.118	

Appendix 1: Testing table

20	0.0091	0.0116	0.0087	0.0110	0.092	
21	0.0201	0.0255	0.0324	0.0411	0.107	0.160
22	0.0076	0.0096	0.0072	0.0091	0.084	
23	0.0175	0.0222	0.0294	0.0373	0.098	0.147
24	0.0101	0.0129	0.0088	0.0111	0.077	
25	0.0166	0.0211	0.0254	0.0322	0.090	0.135
26	0.0105	0.0134	0.0081	0.0103	0.071	
27	0.0151	0.0192	0.0223	0.0283	0.083	0.124
28	0.0051	0.0065	0.0110	0.0139	0.066	
29	0.0131	0.0166	0.0203	0.0257	0.078	0.117
30	0.0012	0.0015	0.0044	0.0056	0.061	
31	0.0113	0.0144	0.0185	0.0234	0.073	0.109
32	0.0015	0.0019	0.0028	0.0035	0.058	
33	0.0102	0.0130	0.0156	0.0198	0.068	0.102
34	0.0025	0.0032	0.0043	0.0055	0.054	
35	0.0095	0.0121	0.0134	0.0171	0.064	0.096
36	0.0036	0.0046	0.0040	0.0051	0.051	
37	0.0080	0.0102	0.0110	0.0140	0.061	0.091
38	0.0023	0.0029	0.0041	0.0052	0.048	

Appendix 1: Testing table

39	0.0087	0.0110	0.0108	0.0138	0.058	0.087
40	0.0022	0.0028	0.0036	0.0045	0.046	
Note: the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.						

Table 5.4.2 Voltage Fluctuations and Flicker				P
	dc(%)	dmax(%)	Running	
Limit	4%	4%	P_{st} = 1.0	P_{lt} = 0.65
Test value	0.039	0.176	0.041	0.029

Table 5.5 and 5.6						P
G83/2 Limit	**DC injection**			**Power factor**		
	0.25%, tested at three power levels			0.95 lag– 0.95 lead at three voltage levels, Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.		
Test level	10%	55%	100%	216.2V	230V	253V
Test value	7.21mA	4.93mA	4.77mA	0.9962	0.9965	0.9885

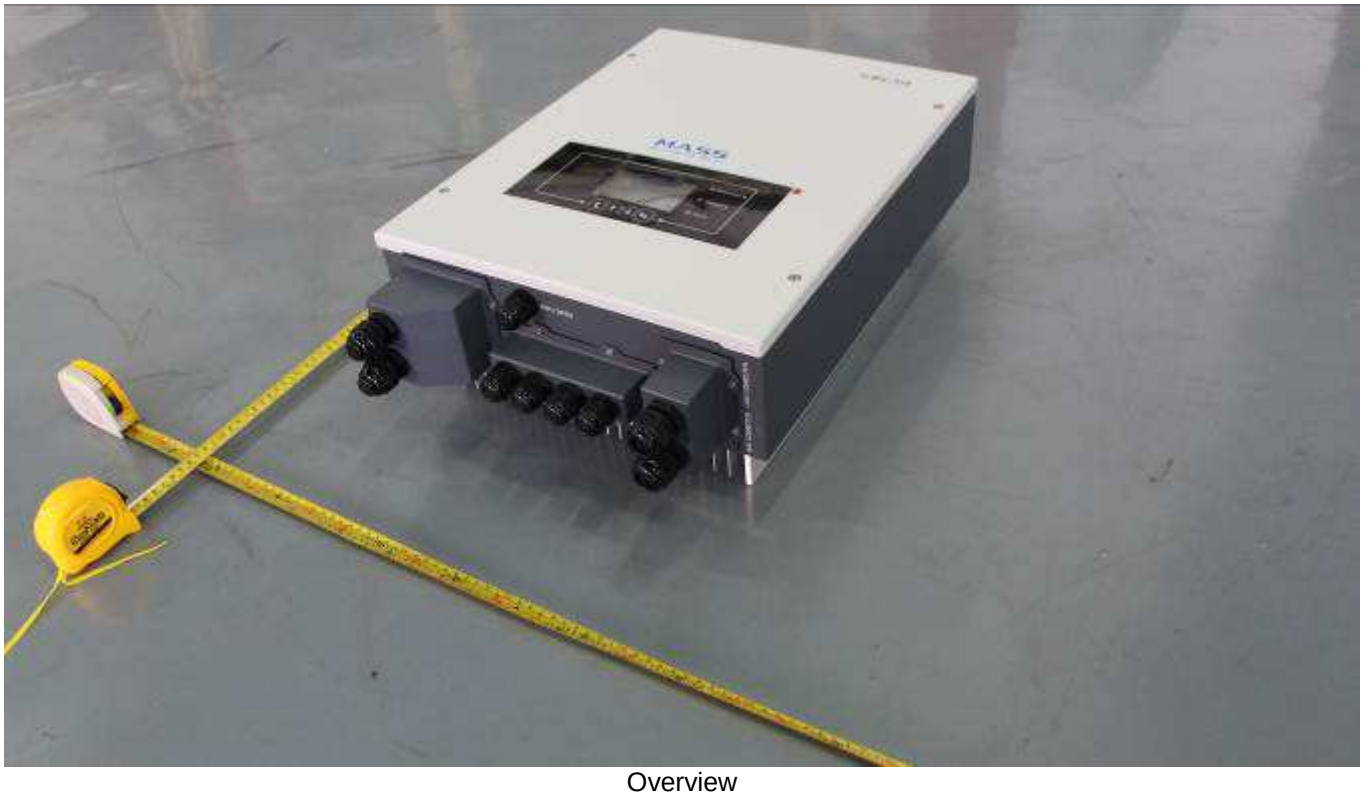
Appendix 1: Testing table

Table 5.7 Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6		
For an Inverter SSEG.		
Time after fault	Volts	Amps
20ms	30.0V	16.9Apeak
100ms	42.0V	16.9Apeak
250ms	--	--
500ms	--	--
Time to trip	218.0ms	

SELF MONITORING – SOLID STATE SWITCHING	
Test	**N/A**
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volt within 0.5 sec.	**No** **(mechanical relays used)**

Appendix 2: Photos

Overview



Overview

Appendix 2: Photos

Top view

Heatsink view

Appendix 2: Photos

Terminal view

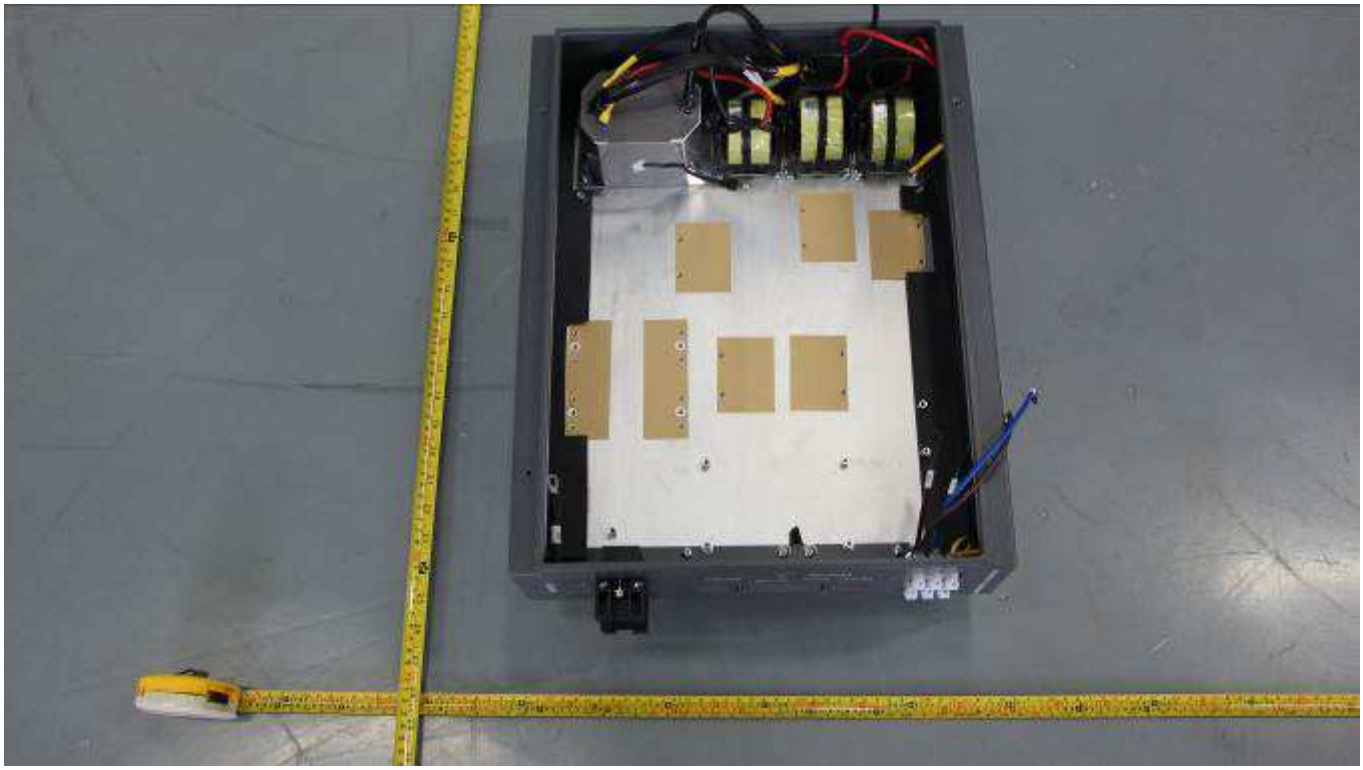
Terminal view

Appendix 2: Photos

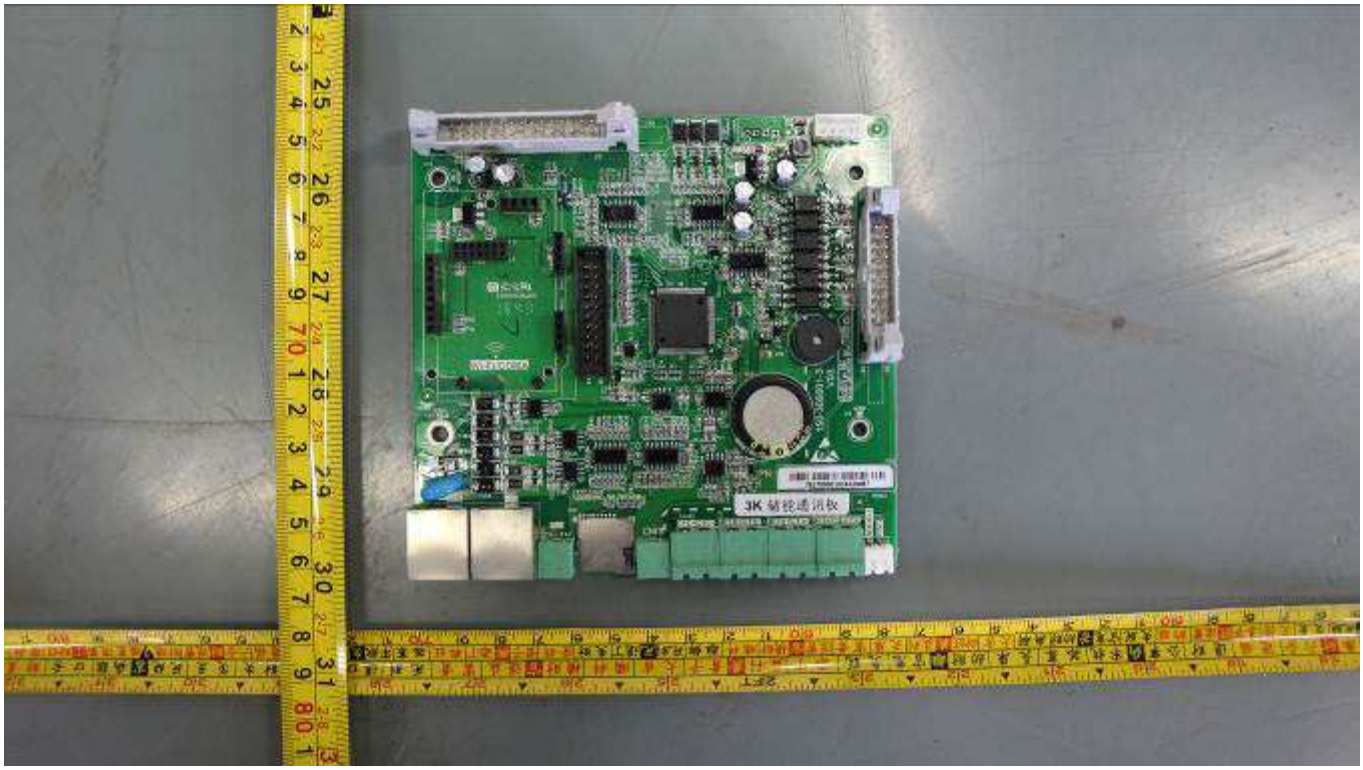
Inside view

Inside view

Appendix 2: Photos

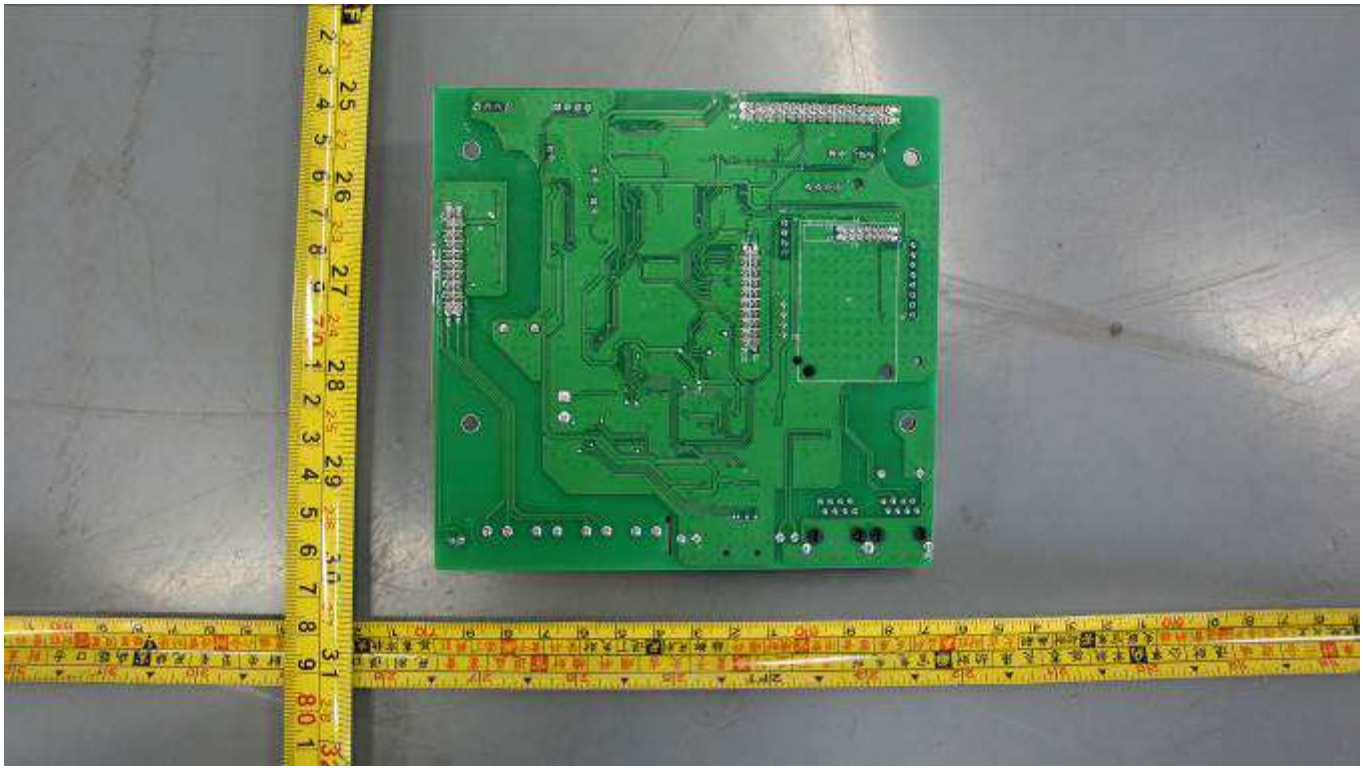


Inside view

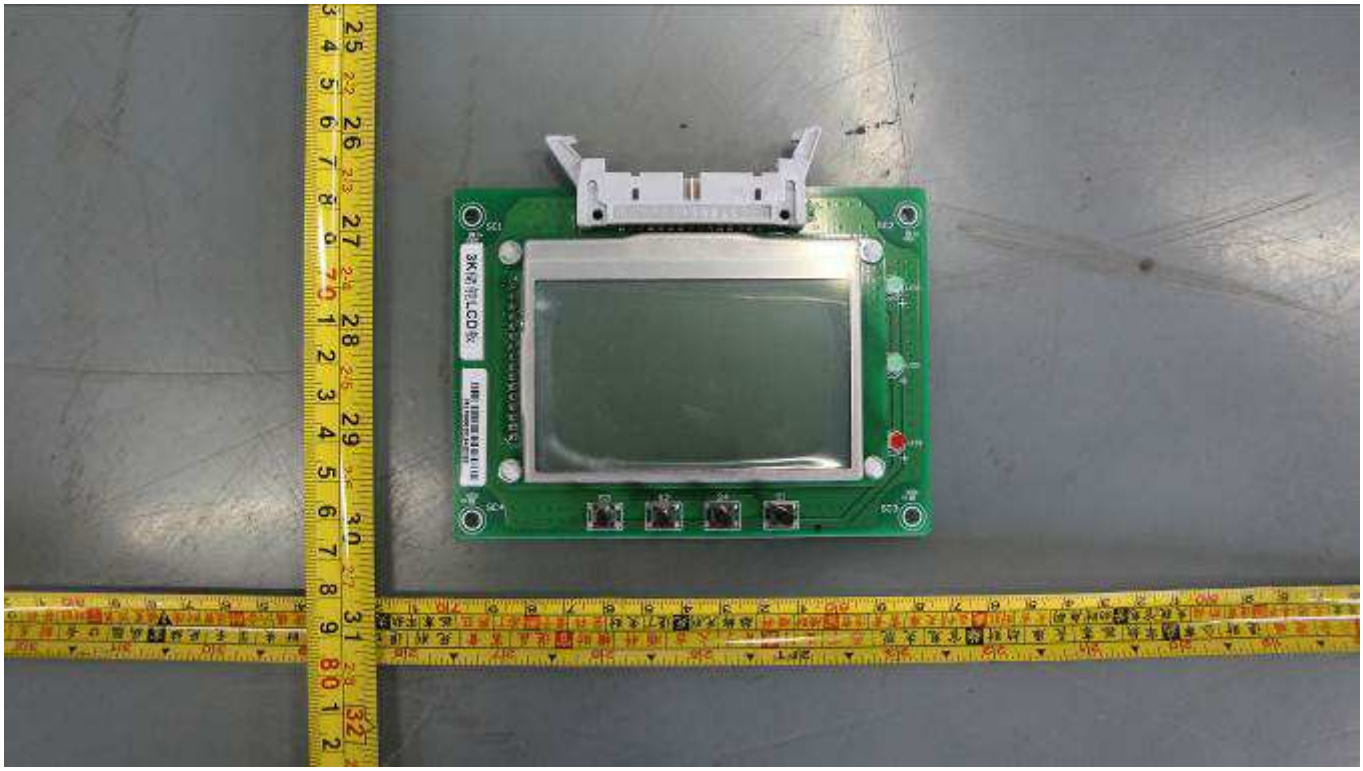


Communication board view

Appendix 2: Photos

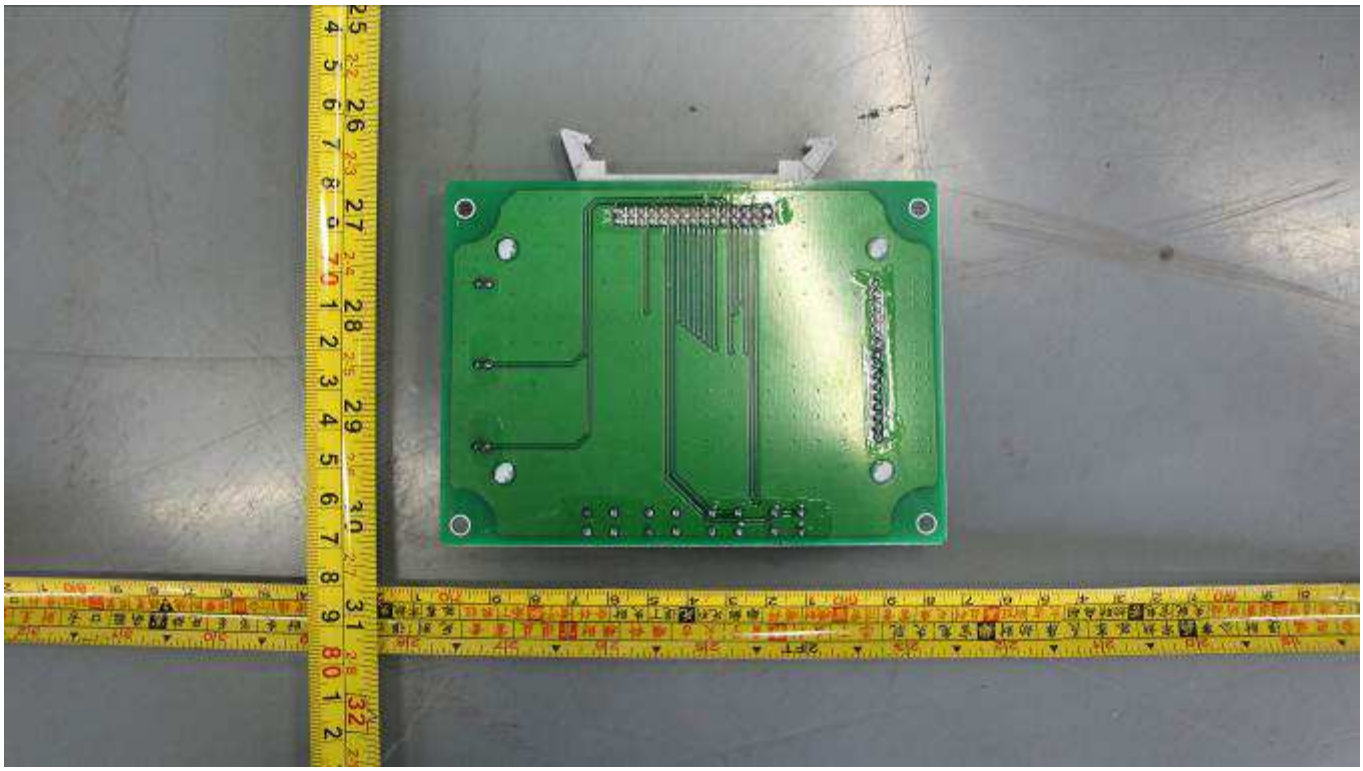


Soldered view

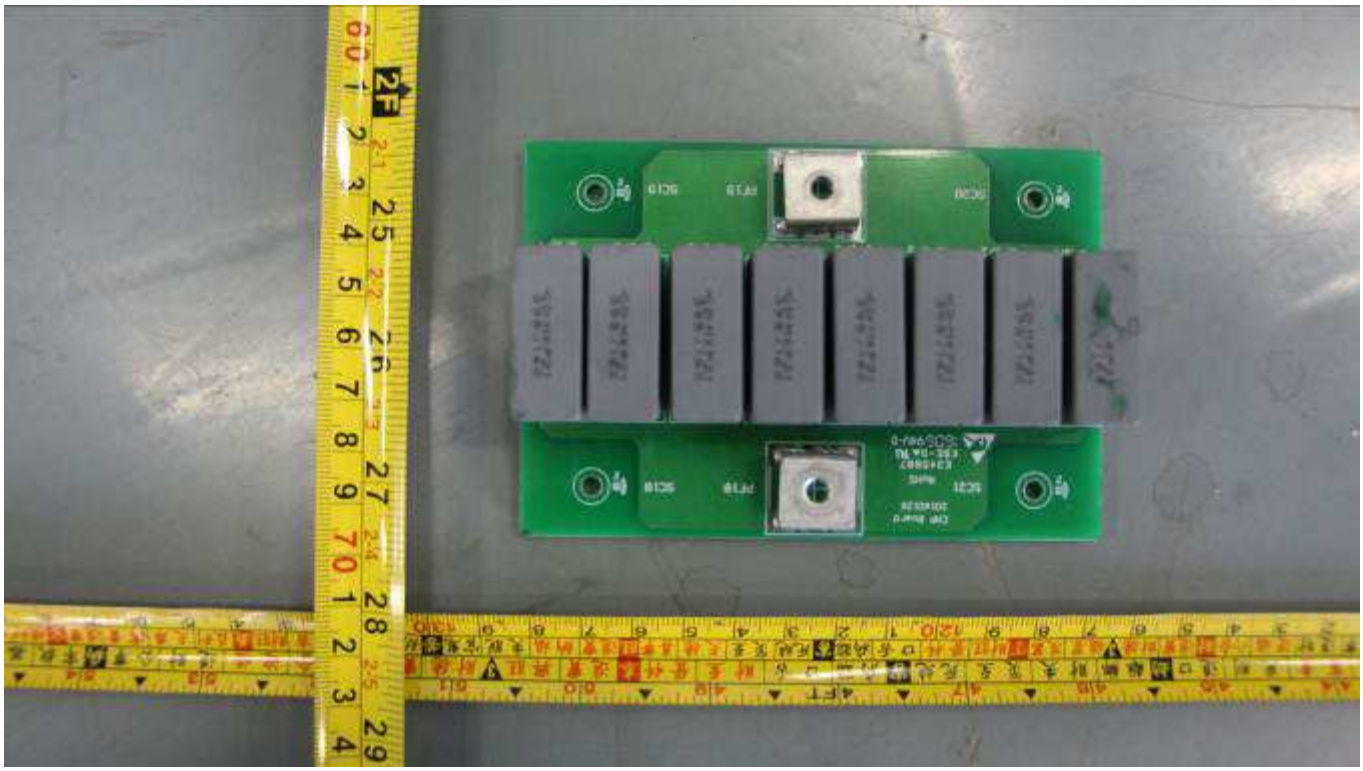


LCD display view

Appendix 2: Photos

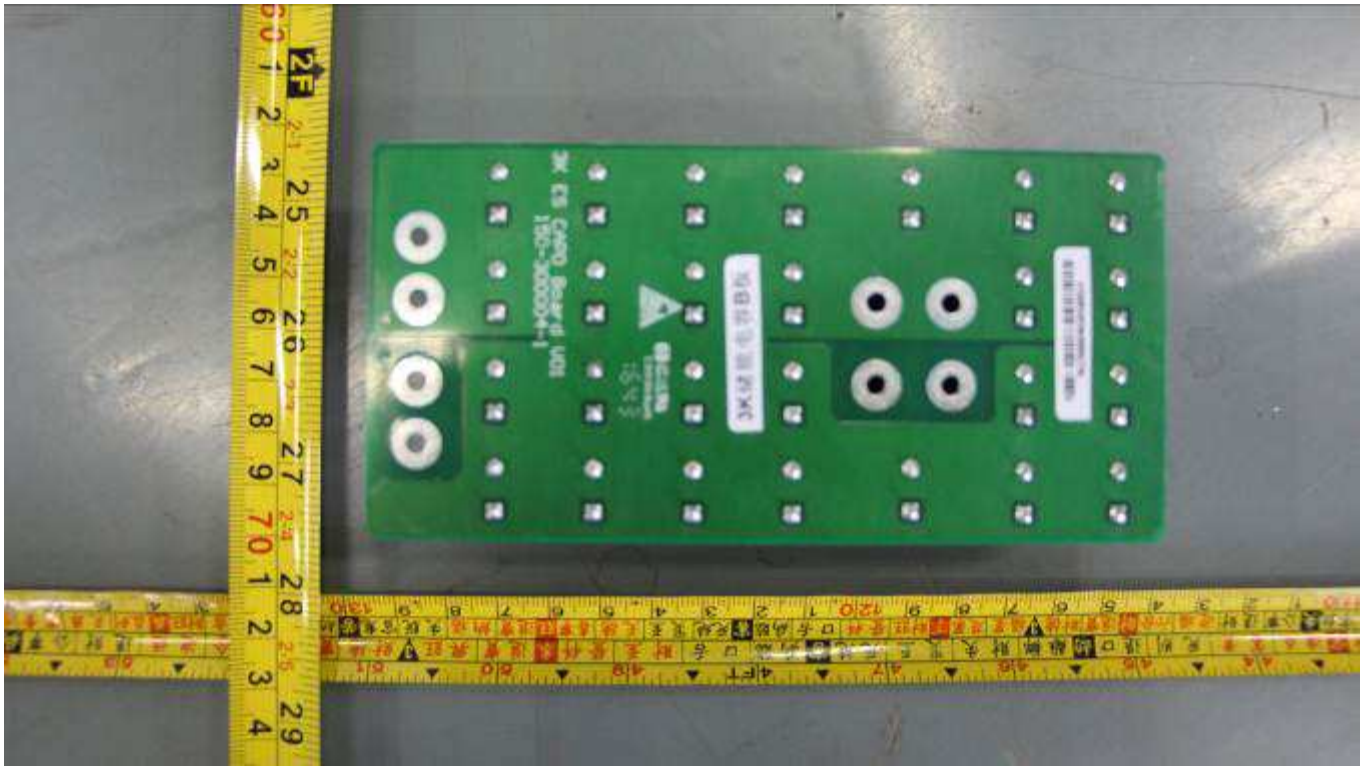


LCD display view



Capacitor A board view

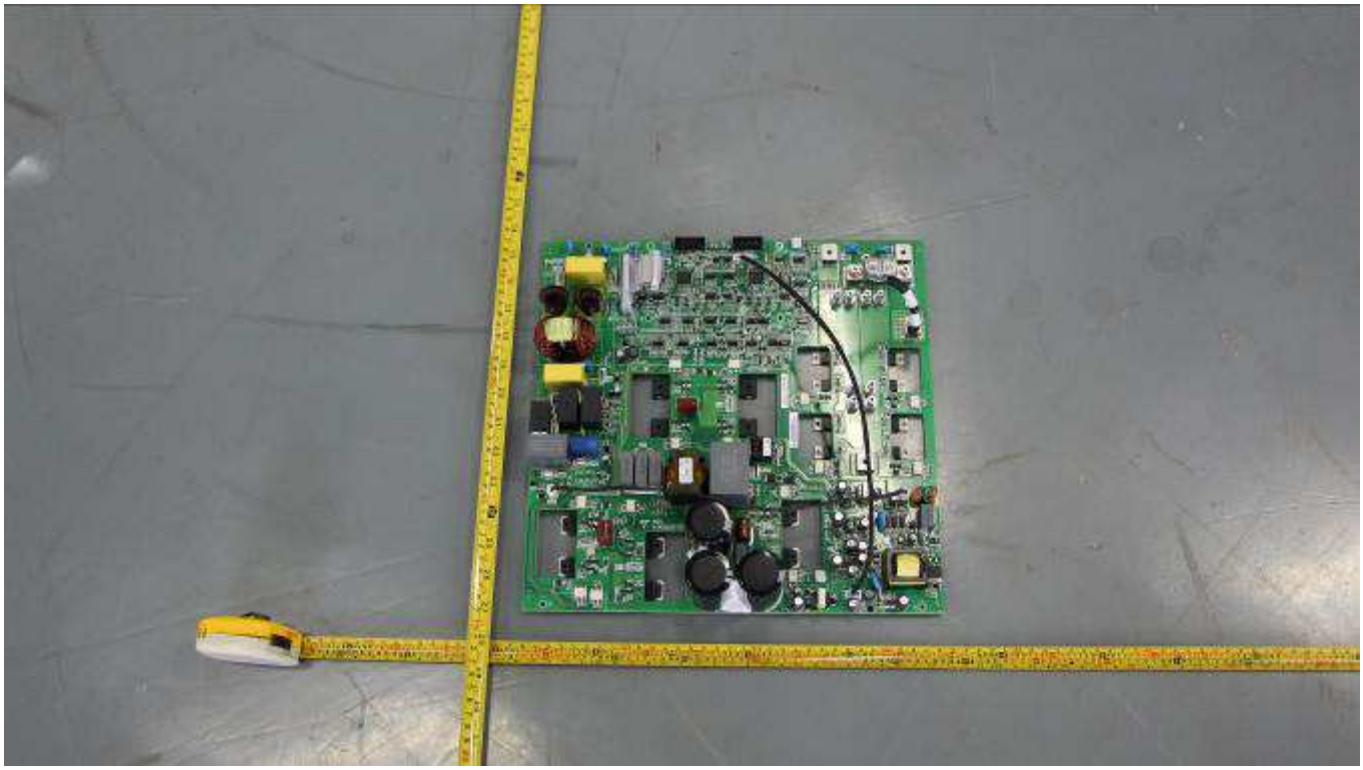
Appendix 2: Photos



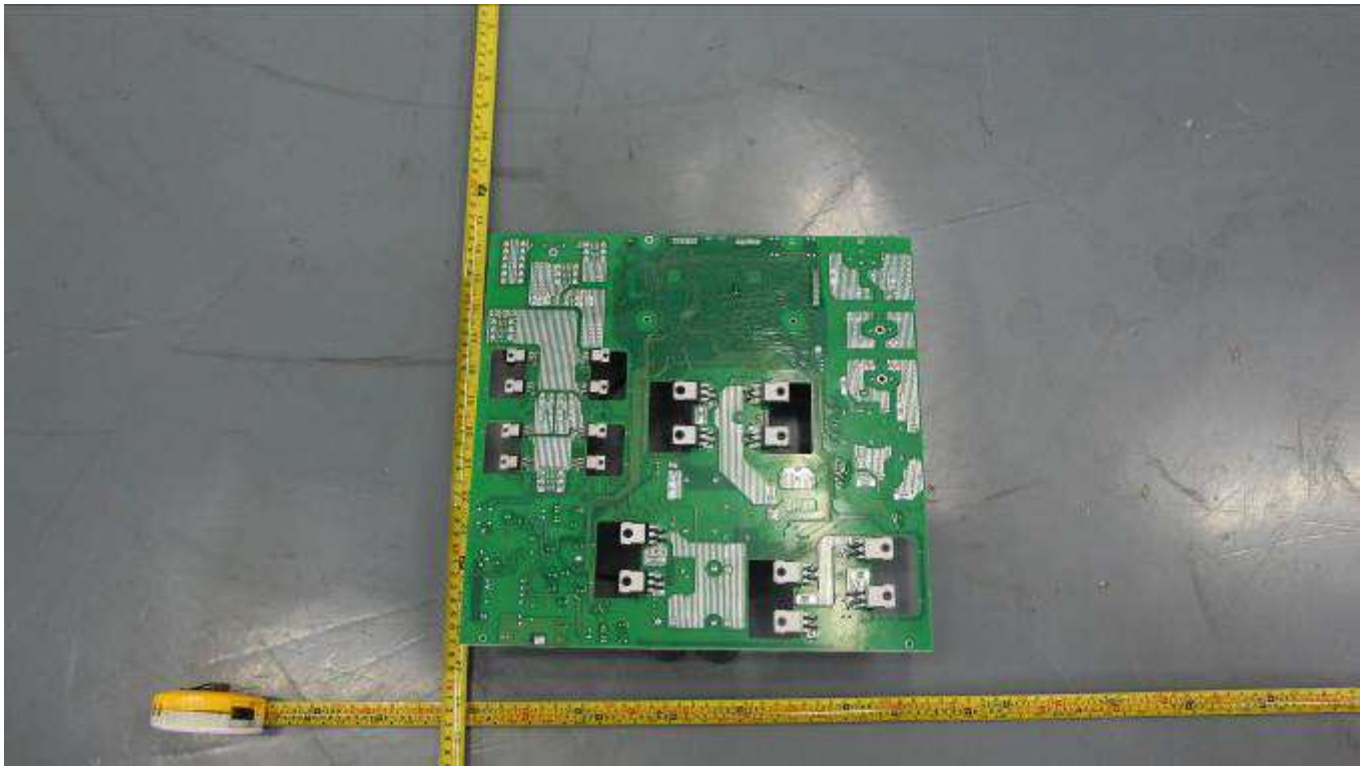
Soldered view

Capacitor B board view

Appendix 2: Photos



Main board view



Soldered view